A Successful Industry Collaboration Model to Achieve Toxics Use Reduction

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November 4, 2009

Lead in Electronics

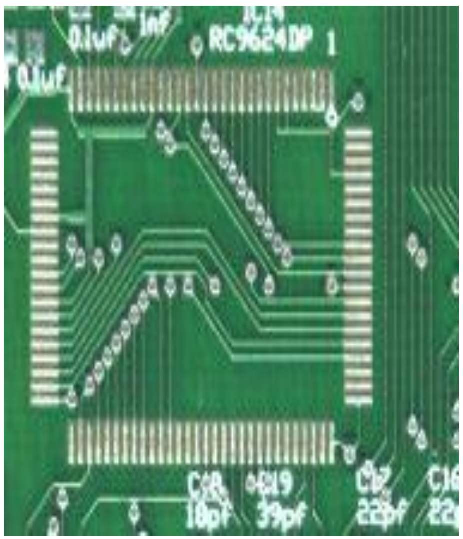
- The printed circuit board is the key component to the manufacture and sales of about $1 trillion in electronic products each year.

- In the United States during 2003, approximately 13.9 million pounds of lead were used for the manufacture of electronics products and the global use of lead materials in electronics approximately 80 – 90 million pounds globally.

Introduction

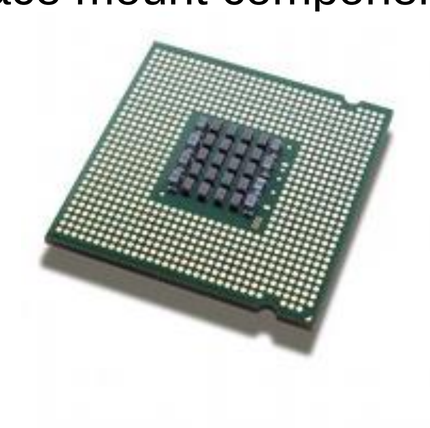
Lead can be used in four major areas on printed circuit boards:

1. Conductive surface finish on circuit board



2. Conductive component finish

Surface mount components (SMT)



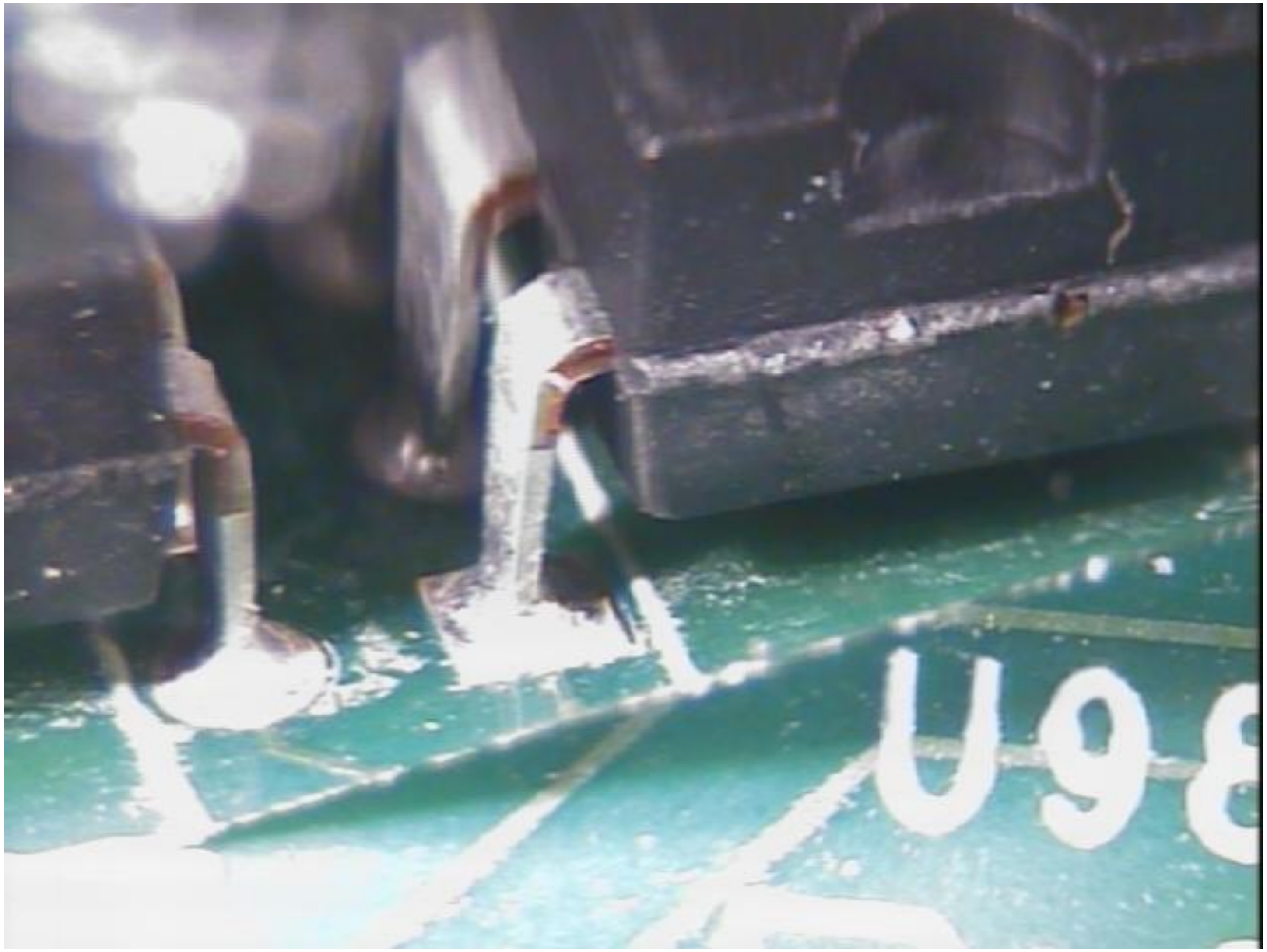
Through hole components (THT)

Introduction

3. Bar solder for assembly of through-hole components

4. Solder paste for the assembly of surface mount components

Lead in Circuit Boards



Human Health Effects

Acute effects of lead exposure:

Brain damage, kidney damage, and gastrointestinal distress occur from acute exposure to high levels of lead in humans. The most sensitive targets for the acute toxic effects of lead are the kidneys and the hematological, cardiovascular, and nervous systems.

Chronic effects of lead exposure:

EPA considers lead to be a Group B2, probable human carcinogen. Chronic exposure to lead in humans can affect the blood, reproductive, and the nervous system.

Human Exposure

Human exposure to lead in electronics typically occurs through a combination of inhalation and oral exposure during manufacturing processes, and during improper disposal at product end-of life.

Lead-free Electronics

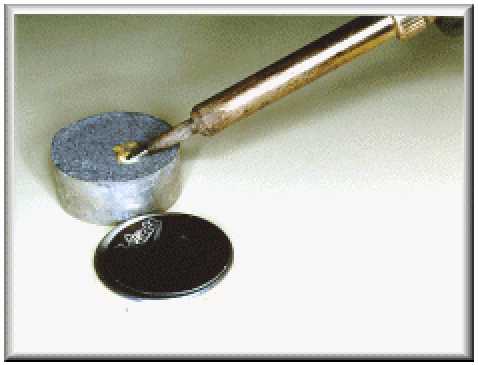
- Global efforts are underway in the electronics industry to initiate a move towards using lead-free materials for the production of printed circuit boards. These efforts are driven by regulatory (i.e. RoHS) and market drivers.

- Numerous technical challenges remain to hinder the universal implementation of lead-free materials, mostly due to the higher melting temperatures of lead-free solders. As a result, most high reliability electronics products are still currently manufactured and assembled using lead materials.

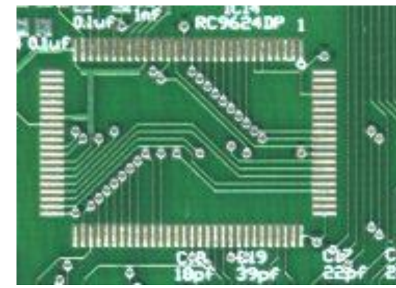



Lead-free Electronics Industry Challenges

1. Which lead-free solders?



2. Which lead-free board finishes?



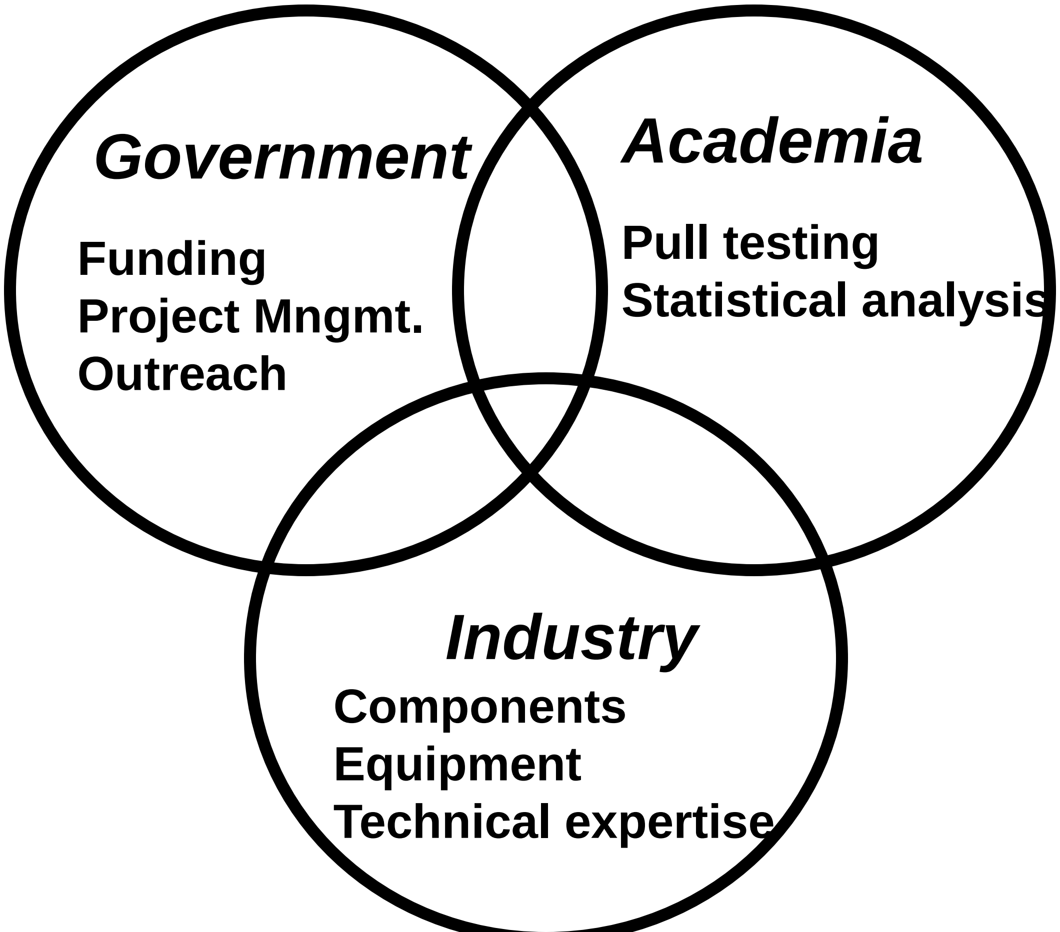
3. Which lead-free component finishes?

4. What process modifications?

Lead-free Electronics Initiatives

- **Company specific initiatives**
- **Industry association sponsored initiatives**
- **Government/academia/industry partnerships**

New England Lead-free Electronics Consortium



Consortium Plan

Objectives:

Design, assemble, and test printed circuit boards using lead-free materials to achieve equal or better solder joint integrity for lead-free electronics assembly as compared to leaded electronics assembly.

Share and disseminate the research results with consortium members as well as the entire electronics industry.

Consortium Members

Project Manager:
Greg Morose, TURI

General Consortium Members

Representatives from industry, government, and academia

Subgroups: Assigned to address specific tasks

- FMEA creation subgroup
- Design subgroup
- Rework subgroup
- Reliability subgroup

Contributions

Contribution	Value
Production equipment and technical support	$90,000
Analysis and project management	$185,000
U.S. EPA funding	$62,000
Engineering support	$240,000
Testing, inspection, and support	$245,000
Components and materials	$195,000
Total	> $1,000,000

Phase IV Contributors

Raytheon
M/A-COM
DDi
isola
TERADYNE
COBHAM
ORMECON
EMC² where information lives®
WALL® Wall Industries, Inc.
Benchmark Electronics
STENTECH
United States Environmental Protection Agency
Texas Instruments
AIM
TURI
Interconnect PWB Solutions Inc.
FREEDOM CAD Services
IOR International Rectifier
UMASS LOWELL
TEXTRON

Consortium Communication

- Bimonthly consortium meetings
- Subgroup meetings (design, rework, reliability)
- Distribution of meeting materials and meeting minutes
- Subgroup documentation and presentation of results
- Surveys
- Workshops and conferences
- Develop papers and articles for submission to electronics publications and electronics conferences
- Presentation at major electronics conferences
- Maintain consortium website

Three Research Areas

- **Assembly**: Assemble SMT and THT components onto printed circuit boards using LF materials with equal or less defects than TL assembly.

  Metric: Defects per unit

- **Rework**: Rework involves the removal and replacement of components onto the printed circuit board due to component defect or wear-out.

  Metric: Level of copper dissolution

- **Long-term reliability**: Address issues for lead-free electronics products requiring long product life.

  Metric: Number of thermal cycles to failure

Six Sigma Approach - DMAIC

Define

- ❑ Initiate the Project
- ❑ Define the Process
- ❑ Determine Customer Requirements
- ❑ Define Key Process Output Variables

Measure

- ❑ Understand the Process
- ❑ Evaluate Risks on Process Inputs
- ❑ Develop and Evaluate Measurement Systems
- ❑ Measure Current Process Performance

Analyze

- ❑ Analyze Data to Prioritize Key Input Variables
- ❑ Identify Waste

Improve

- ❑ Verify Critical Inputs Using Planned Experiments
- ❑ Design Improvement
- ❑ Pilot New Process (Implement)

Control

- ❑ Finalize the Control System
- ❑ Verify Long Term Capability

Problem Solving Approach

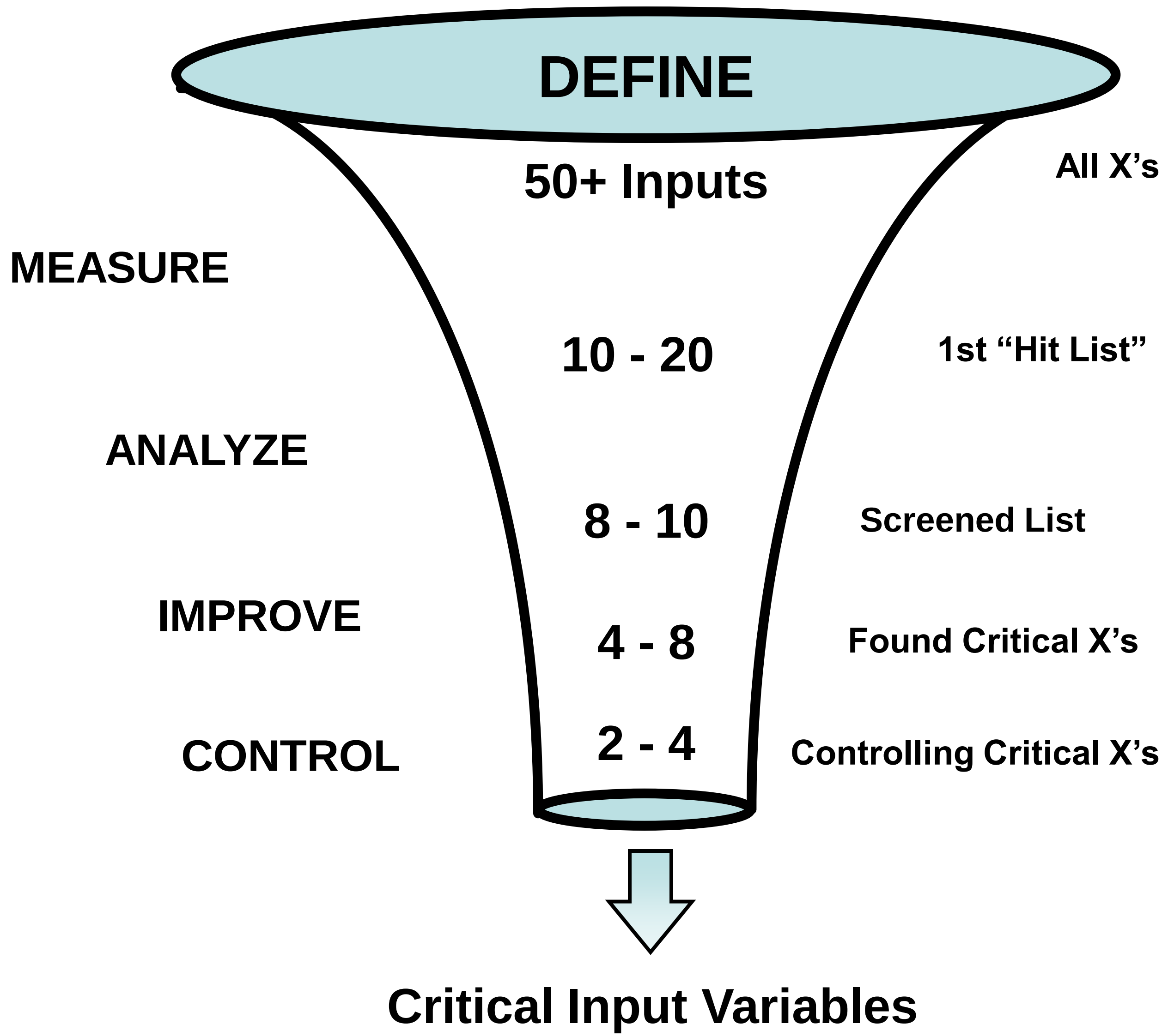
Our Key Process Output Variables (Y's) are determined by our KPIVs (X's). If we know enough about our X's we can accurately predict Y.

$$Y = f(x_1, x_2, x_3, \ldots, x_k)$$

Y1: Defects per unit (assembly)
Y2: Copper dissolution (rework)
Y3: Cycles to failure (reliability)

(Y1) Solder joint integrity/DPU = (reflow profile, solder material, print speed, surface finish, component finish, laminate material, dwell time, solder pot temperature, etc.)

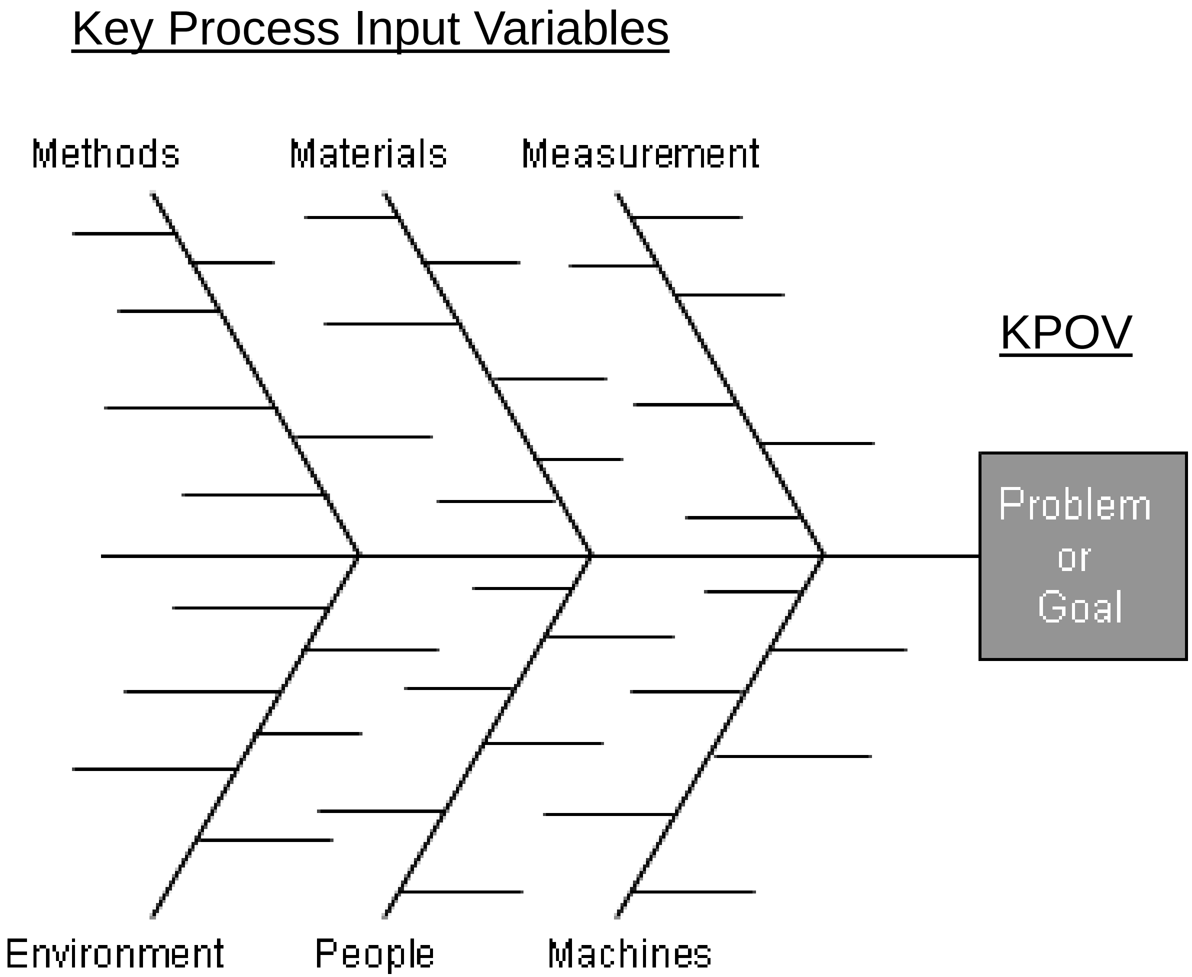
Determine Critical Inputs



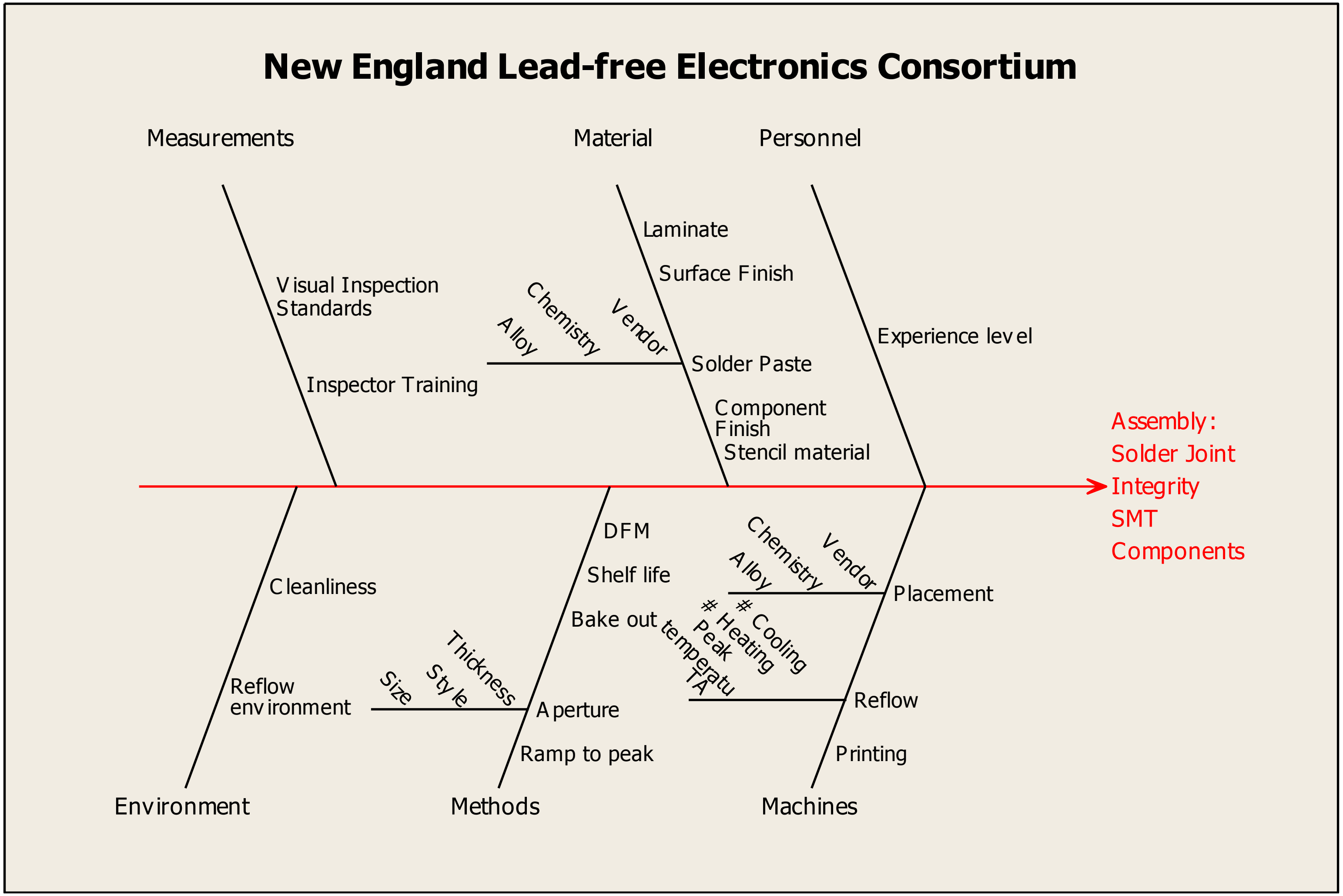
Methods Used to Reduce X’s

- Phase I, II, and III experiment results
- Surveys and meetings with technical experts
- Cause and Effect diagrams
- Failure Modes and Effects Analysis (FMEA)

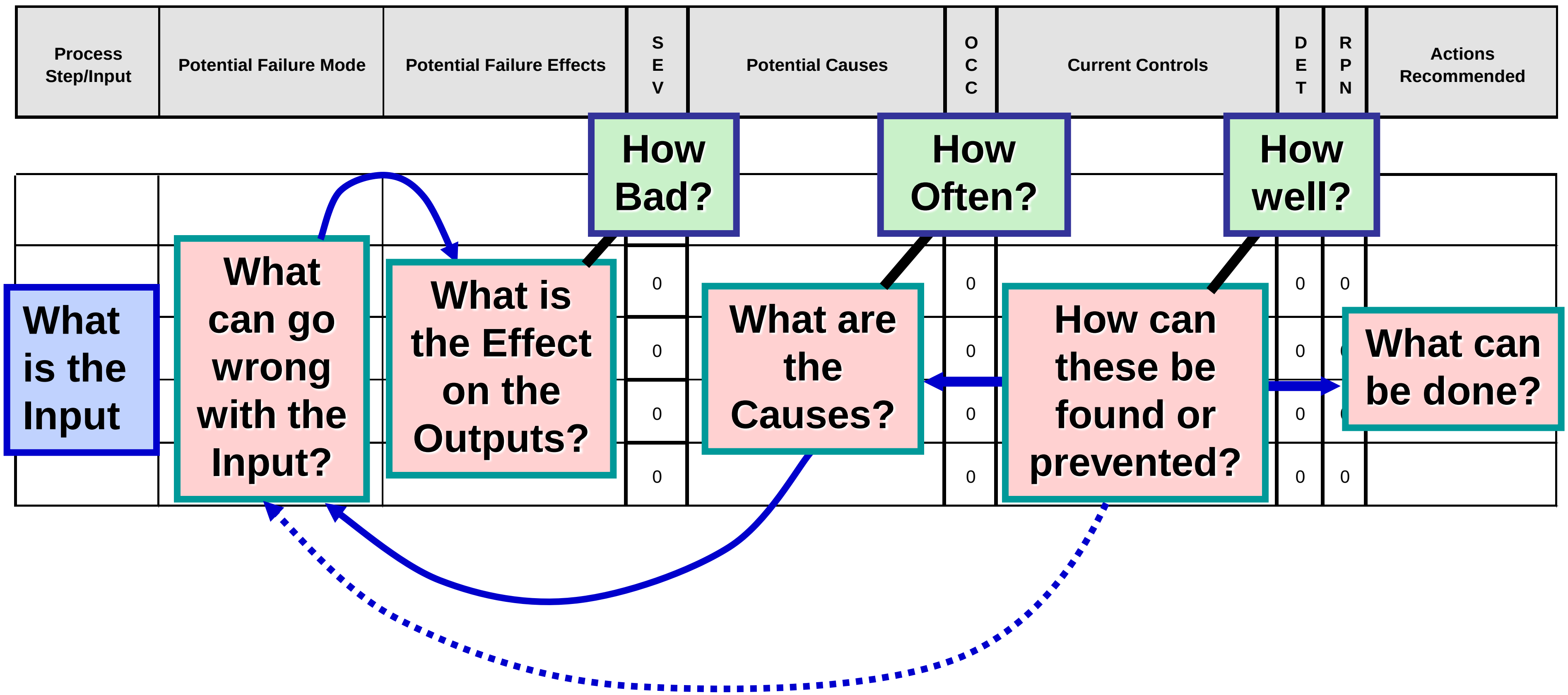
Cause and Effect Diagram



Cause and Effect Diagram



FMEA Overview



Risk Priority Number (RPN)

- The RPN is an output of FMEA
- The RPN is used assist in the prioritization of items in the FMEA based on three characteristics
  - Severity of the Effects
  - Occurrence of the Causes
  - Detection capabilities of current Controls

RPN = Severity X Occurrence X Detection

Effects — Causes — Controls

Simple Rating Scale

Rating	Severity of Effect	Likelihood of Occurrence	Ability to Detect
10	Lose Customer	Very high: Failure is almost inevitable	Can not detect
9	Serious impact on customer's business or process		Very remote chance of detection
8	Major inconvenience to customer	High: Repeated failures	Remote chance of detection
7	Major defect noticed by most customers		Very low chance of detection
6	Major defect noticed by some customers	Moderate: Occasional failures	Low chance of detection
5	Major defect noticed by discriminating customers		Moderate chance of detection
4	Minor defect noticed by most customers		Moderately high chance of detection
3	Minor defect noticed by some customers	Low: Relatively few failures	High chance of detection
2	Minor defect noticed by discriminating customers		Very high chance of detection
1	No effect	Remote: Failure is unlikely	Almost certain detection

FMEA Page 1 of 5

Item No: Lead Free Solder Process	Process Responsibility: TURI Lead Free FMEA Group		FMEA No: FMEA0100	Page: 1/5
Core Team: TURI Lead Free Group	Issue Date: September 20, 2006	Revision: 9/13/06	Customer: Lead Free Process	

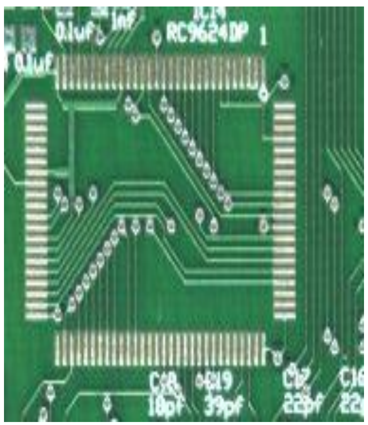
FMEA No / Process										Follow Up						
No	**Failure Mode**	**Cl**	**Effect**	**Sev**	**Cause**	**Occ**	**Process Controls**	**Det**	**RPN**	**Planned Actions**	**Date**	**CAR**	**Sev**	**Occ**	**Det**	**RPN**
Screen Printing																
002	Insufficient Pad Coverage per IPC-610 Rev D		Poor print (Insufficient height, Volume)	8	Incorrect aperture size on stencil/Stencil thickness/Equipment parameter print set up	6	AOI/Monitoring paste shelf life/Monitor Solder paste exposure time/Maintenance of the equipment/LSM paste measurements height, volume, Visual Inspection	5	**240**	Process Owner Specific			8	3	3	**72**
034	insufficient solder		Poor Print	8	improper precondition of paste/Paste sticking to stencil/Poor Print Parameters;	6	AOI/Monitoring paste shelf life/Monitor Solder paste exposure time/Maintenance of the equipment/LSM paste measurements: height, volume/visual inspection	5	**240**	Process owner specific			8	3	3	**72**
035	improper solder print dispensing		Poor print	7	paste problems: clogged tube/old paste/	5	AOI/Monitoring paste shelf life/Monitor Solder paste exposure time/Maintenance of the equipment/LSM paste measurements height, volume, visual Inspection	5	**175**	Process owner specific			7	3	2	**42**
Pick & Place																
004	components fail AOI system with lead free soldering. Balls not seen.		Component rejection (false rejection)	3	vision system not optimized for lead free	7	Optimize Machine for lead free soldering.	2	**42**	Process owner specific			3	1	2	**6**
Reflow																
023	Ceramic ball grid array solder joint failure/cracking		test failure/latent failures	8	CTE mismatch/Poor CBGA Design/	8	Review CBGA design/Reliability Qualification	9	**576**	Process Owner Specific			8	4	9	**288**
028	excess Intermetallic growth		weak solder joint/environmental failure	10	HASL/ Sn Plating with SnCu Ni barrier prevents excess IMC or electroimmersion sn, improper reflow profile	8	Material selection , nickel barrier between tin and copper, witness part analysis, proper reflow profile	10	**800**	Process Owner Specific			10	2	10	**200**

Critical X's

LF Solder paste alloys: Numerous	SAC305
Atmosphere: air, nitrogen	Air
Thermal profile: soak, ramp/peak	Ramp/peak
LF THT Solder: Numerous	SAC305, Sn100C
Laminate material: Numerous	2 laminates
Surface finish: Numerous	4 finishes

Lead-free Materials

1. Conductive surface finish on circuit board

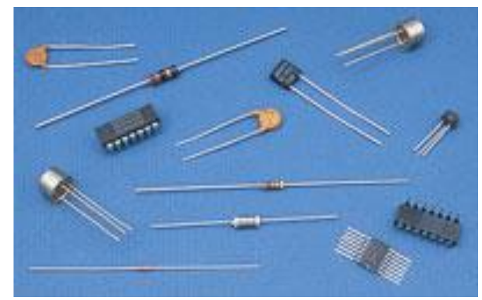


- ENIG (nickel, gold)
- OSP (copper)
- Nano (nanosilver, polyaniline)
- HASL (tin/copper alloy)

2. Conductive component finish

Surface mount components (SMT)

Through hole components (THT)



- NiPdAu (nickel/palladium/gold)
- Sn (tin)
- Au (gold)
- SnAgCu (tin/silver/copper)
- SnBi (tin/bismuth)

Lead-free Materials

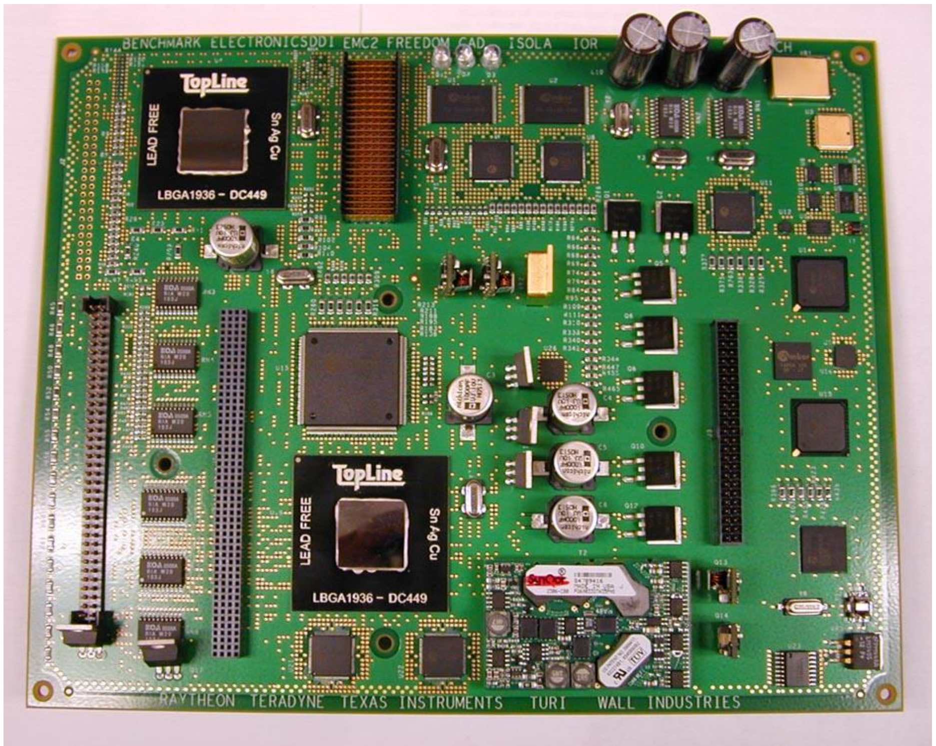
3. Bar solder for assembly
of through-hole components

- Tin/copper (Sn100C)
- Tin/silver/copper (SAC305)

4. Solder paste for the assembly
of surface mount components

- Tin/silver/copper (SAC305)

Test Vehicle



Test Vehicle

- 8” wide x 10” long
- 20 layers
- 0.110 inches thick
- 907 components per test vehicle

SMT Components:
Resistors, BGAs, microBGAs, PQFN, TSSOP, PQFP, MLF, Transformer

THT Components:
Connectors, LEDs, capacitors, DC/DC Convertors, TO220

DOE for Through Hole Component Assembly Results

Y1: Defects per unit (assembly)

X1: Through hole solder (4 different solder/process settings)
X2: Surface finish (4 different types)

Design of Experiments:
- Full factorial
- 2 replicates
- 2 factors (through hole solder, surface finish)
- 2 replicates x 4 levels of solder x 4 levels of surface finish = 32 test vehicles (runs)

Design of Experiments

Lead-free Test Vehicles

Board	SMT Solder Paste	Through Hole Solder	Surface Finish
1	SAC305 NC-1	SAC305	ENIG
2	SAC305 NC-1	SAC305	ENIG
3	SAC305 NC-1	SAC305	LF HASL
4	SAC305 NC-1	SAC305	LF HASL
5	SAC305 NC-1	SAC305	OSP
6	SAC305 NC-1	SAC305	OSP
7	SAC305 NC-1	SAC305	Nanofinish
8	SAC305 NC-1	SAC305	Nanofinish

Design of Experiments

Lead-free Test Vehicles

Board	SMT Solder Paste	Through Hole Solder	Surface Finish
9	SAC305 (OA)	Sn100C-1	ENIG
10	SAC305 (OA)	Sn100C-1	ENIG
11	SAC305 (OA)	Sn100C-1	LF HASL
12	SAC305 (OA)	Sn100C-1	LF HASL
13	SAC305 (OA)	Sn100C-1	OSP
14	SAC305 (OA)	Sn100C-1	OSP
15	SAC305 (OA)	Sn100C-1	Nanofinish
16	SAC305 (OA)	Sn100C-1	Nanofinish

Design of Experiments

Lead-free Test Vehicles

Board	SMT Solder Paste	Through Hole Solder	Surface Finish
17	SAC305 NC-2	Sn100C-2	ENIG
18	SAC305 NC-2	Sn100C-2	ENIG
19	SAC305 NC-2	Sn100C-2	LF HASL
20	SAC305 NC-2	Sn100C-2	LF HASL
21	SAC305 NC-2	Sn100C-2	OSP
22	SAC305 NC-2	Sn100C-2	OSP
23	SAC305 NC-2	Sn100C-2	Nanofinish
24	SAC305 NC-2	Sn100C-2	Nanofinish

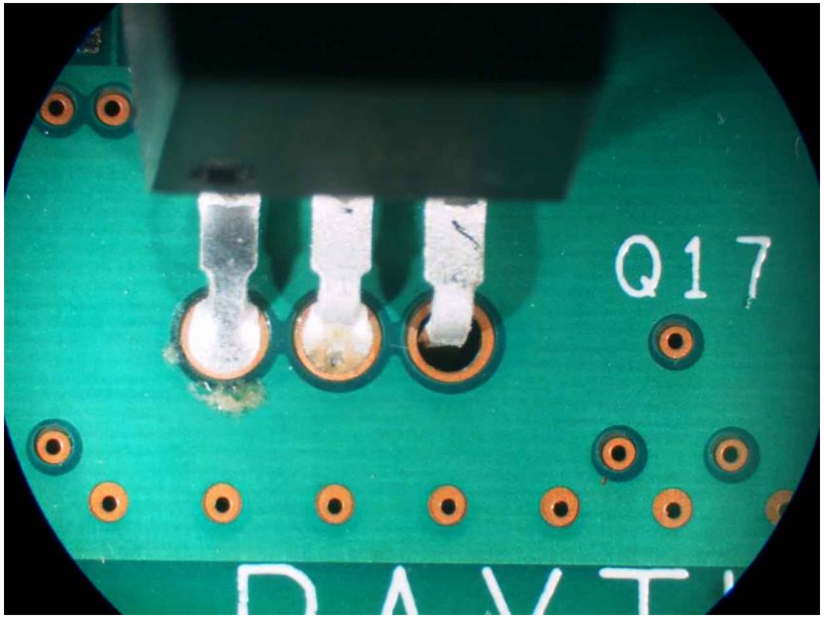
Design of Experiments

Tin/lead Test Vehicles

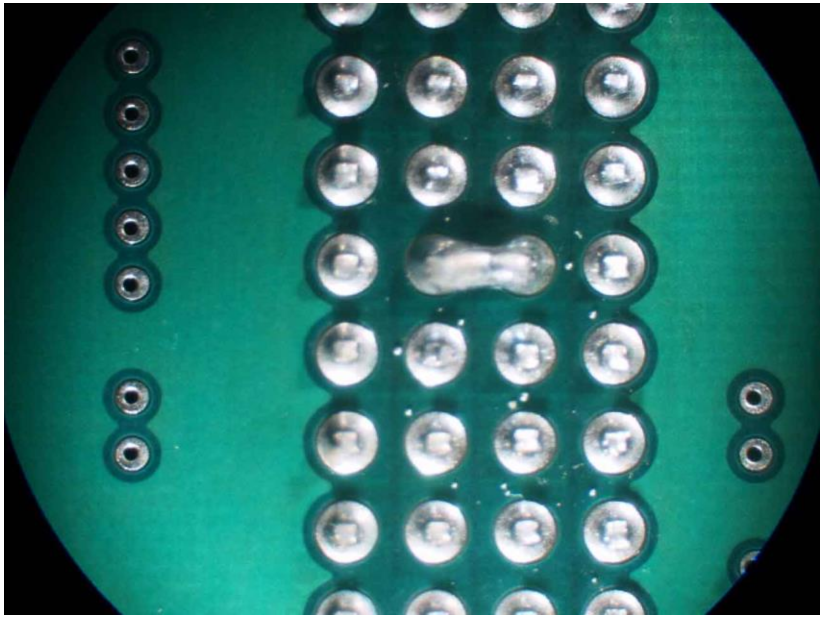
Board	SMT Solder Paste	Through Hole Solder	Surface Finish
25	Tin/lead NC	Tin/Lead	ENIG
26	Tin/lead NC	Tin/Lead	ENIG
27	Tin/lead NC	Tin/Lead	LF HASL
28	Tin/lead NC	Tin/Lead	LF HASL
29	Tin/lead NC	Tin/Lead	OSP
30	Tin/lead NC	Tin/Lead	OSP
31	Tin/lead NC	Tin/Lead	Nanofinish
32	Tin/lead NC	Tin/Lead	Nanofinish

THT Defects

Tin/lead and Lead-free: Most common defects were insufficient solder and solder bridge

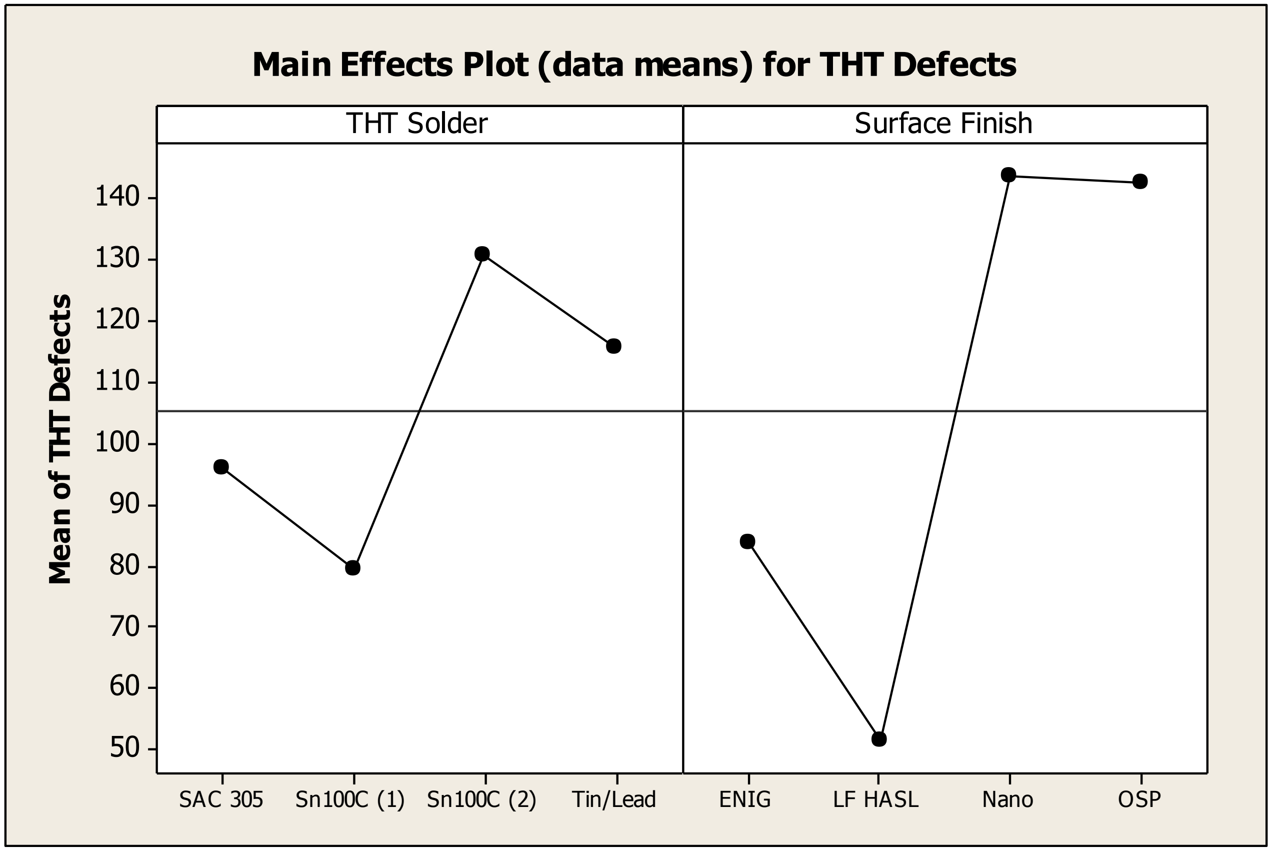


TO220, Insufficient solder, Test vehicle 22, Q17



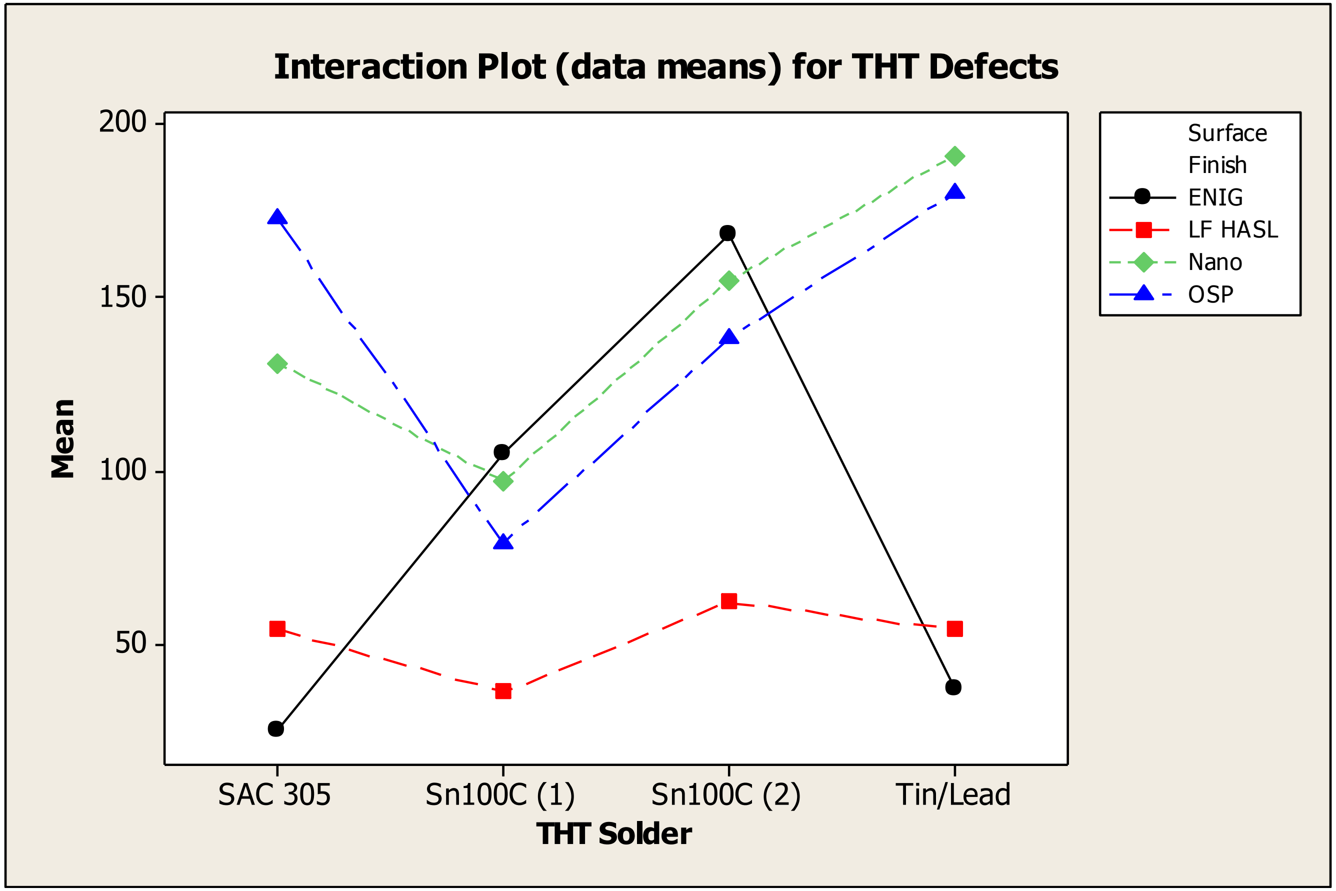
200 pin connector, Solder bridge, Test vehicle 28, J5

Assembly Results: THT Component Main Effects



- Sn100C (1) had the lowest defect rate for all solders
- Lead-free HASL had the lowest defect rate for all surface finishes

Assembly Results: THT Component Interaction



- ENIG surface finish had the lowest defects with SAC305 and tin/lead solders, but had the highest defect rate with Sn100C solder (both settings)
- LF HASL had a low defect rate for each of the four solder types

Consortium Accomplishments

Demonstrated Success:

Demonstrated that lead-free electronics assembly and rework can be done with equal or fewer defects than tin/lead assembly for SMT. Long-term reliability research is still underway.

Leveraged Resources:

Collaborated to share the cost and resources necessary to design, build, and test numerous experimental PCBs

Outreach Beyond Consortium Members:

- Articles
- Technical papers
- Conference and workshop presentations

Consortium Member Benefits

Academia:

Forged collaborative relationships between university and regional businesses.

Provided real world learning opportunities for graduate and undergraduate students.

Increased university faculty experience in applied science and engineering.

Consortium Member Benefits

Government

Reduced the use of a toxic material (lead) which leads to a safer occupational setting and an improved environment.

Improved the competitive position of local businesses by addressing industry challenges in a proactive and efficient manner.

Consortium Member Benefits

Industry

Ability to have input and influence on consortium efforts (e.g. material selection, supplier selection, testing strategies, etc.).

Access to cutting edge research and analysis.

Ability to share the costs to address a major industry challenge.

Forum provided to share ideas and receive advice from industry peers.

Ability to derive competitive advantage for early preparedness.

Individual: Become a knowledge leader within organization.

Thank you.

For any questions, contact:

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