Reliability Testing Results of Surface Mounted Lead Free Soldering Materials and Processes

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Abstract
The world-wide movement to phase out lead from electronic products presents many challenges for companies throughout the electronics supply chain. The University of Massachusetts at Lowell has brought together many Massachusetts/New England firms to collaborate on the manufacture and testing of lead-free printed wiring boards (PWBs). The results of the first set of experiments, published in 2001, showed that zero-defect soldering is achievable with lead-free materials. Following thermal cycling, the PWBs were visually inspected and the leads were pull-tested for reliability analysis. They compared favorably to a baseline of lead soldered PWBs

A follow-on design of experiments was created in 2002 and a second set of test PWBs was made and tested in 2003. Three lead-free solder pastes based on Sn/Ag/Cu alloys were reflowed using either air or nitrogen with five PWB surface finishes, four component types with two types of component finish. Visual inspection and pull-testing were performed and published as completed in APEX, SMTI and IEEE conferences. This paper summarizes the testing results and introduces further research plans in volume manufacturing of lead free PWBs for the phase III testing sponsored by the EPA.

Key words: Lead Free, Visual testing, Reliability testing, Thermal Cycling, Design of Experiments.

Introduction
In January 2003, The European Union published Directives 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE) and 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS). These emerging directives have been the primary drivers for global movement toward lead-free electronics. The RoHS prohibits products that contain lead to be sold in the EU after July 2006, unless the use is specifically exempted.

Massachusetts lead-free consortium
The Massachusetts Toxics Use Reduction Act (TURA) program has a mission to assist companies in reducing or eliminating the use of toxic substances where possible, and in reducing the amount of toxic waste generated. TURA also has a goal "to sustain, safeguard and promote the competitive advantage of Massachusetts businesses, large and small, while advancing innovation in toxic use reduction and management." These goals come together as we assist firms in meeting international materials restrictions on lead in electronic products.

TURI (Toxics reduction Institute) and UML (UMass Lowell) were the primary movers of the consortium to provide training, information, and conduct research in innovative technologies. In 1999, TURI began supporting research at UMass Lowell to investigate alternative lead-free solder processes.

The Massachusetts Lead-Free Research Consortium was formed in 2000, consisting of at least one representative of each part of the electronics supply chain. Members contribute time, materials, facilities, funding and expertise as they jointly develop and implement testing plans. Consortium members and their companies are listed as co-authors in this paper. In 2004, many other companies were added from the New England region, and the consortium changed its name to the New England Lead Free Consortium

In addition to supporting the consortium, TURI periodically brings together firms from the electronics supply chain to exchange information, to communicate the latest technical and regulatory developments, and to report on the consortium's research program (for summaries of papers and presentations, see TURI's web site: www.turi.org).

Experimental design, including factor and level selection, phase ii

A design of experiment matrix was selected by the consortium members based on their collective experience and the available resources and materials. The factors and levels selected were:

1. PWB Finishes
    a. Solder Mask Over Bare Copper with Hot Air Solder Leveled (SMOBC/HASL)
    b. Organic Solder Preservative (OSP)
    c. Electroless Nickel Immersion Gold (ENIG).
    d. Matte Tin (Sn) Electroplate
    e. Immersion Silver (Ag)
2. Reflow Atmospheres
    a. Air
    b. Nitrogen. (Nitrogen was supplied by Air Products and Chemicals and contained 50 ppm Oxygen)
3. Solder Pastes all 95.5Sn-3.8 Ag-0.7Cu (NEMI recommended) from three different suppliers (A, B and C), all incorporating no-clean fluxes. Flux formulations proprietary according to each supplier.
4. Component Lead Finishes
    a. matte tin, Tin plating, Tin/Silver/Copper, Nickel/Palladium/ Gold (NiPdAu), and Nickel/Gold.
    b. tin/silver/copper balls for BGA
5. Sn-Pb eutectic solder PWB using the solder treatments as control PWBs.

Test vehicles and experimental plans, phase II

The test vehicle was a 6" x 9" FR4 board, shown in the pull test fixture (Figure 1). A total of 100 PWBs were assembled and tested. The PWBs were divided as follows:

1. 60 PWBs - 2 sets of 30 to harness the full factorial experiment of 5 finishes, 3 solder suppliers and 2 atmospheres (5 x 3 x 2 = 30). The full factorial experiment is shown in Table 1.
2. 10 PWBs, - 2 sets of 5 PWBs soldered with a leaded solder from supplier B to act as baseline comparison to unleaded solder.
3. 8 PWBs, - 2 sets of 4 to test out a higher concentration of oxygen(50 ppm versus 5000 ppm oxygen)
4. 20 PWBs, - 2 sets of 10 PWBs, to compare the results of leaded and unleaded components versus leaded and unleaded solders, using all 5 PWB finishes, air soldering environment and solder supplier B. This set was performed to demonstrate whether it is possible to exchange unleaded components with leaded components at will in all soldering environments. It is a measure of backward (back and forward compatibility of components compatibility).

Components, phase II

The control PWBs were built with devices that had a tin/lead component finish and the experimental test boards were assembled with parts that had lead-free finishes. The lead-free passive chips were tin-plated and the lead-free integrated circuit devices were plated, some with matte tin, NiPdAu, and nickel/gold. The BGA components had tin/silver/copper solder balls, Components were donated from consortium companies.

Each PWB (shown in Figure 1) included:

1. Standard SMT resistor and capacitor parts. (401 and 402 styles).
2. A set each of 0.030 and 0.014 vias
3. 3 QFP 176 high-density interconnection (HDI) package one with daisy chain terminations,
4. 2 BGA types, 35 and 45 mm
5. 3 SOIC 20 packages, one with daisy chain terminations
6. 3 special IC's used in wireless applications

All components were soldered to the test PWBs using the production facility at Schneider Electric in Andover, MA.

Experiment layout, phase II

The test PWB was laid out at M/A-COM taking into account daisy chain resistance test capabilities in some of the parts and fabricated by Sanmina-SCI with the five different finishes. Pastes were obtained from three vendors and a reflow profile was developed based on the manufacturers' product data sheets. A reflow profile board was populated with parts and three K-probe thermocouples (TC) were attached to the surface. One TC was attached at the leading edge of the PWB, one at the lead attach area of a large QFP and one near the trailing edge. All three manufacturers recommended a 'ramp to spike' curve, shown in Figure 2. Several runs were performed to ensure consistent performance.

Table 1: Lead Free Solder test plan, Phase II

Exper-iment #	Surface Finish	Solder paste	Atmo-sphere
1	(1) SMOBC/HASL	"A"	Air
2	(1) SMOBC/HASL	"A"	Nitrogen
3	(1) SMOBC/HASL	"B"	Air
4	(1) SMOBC/HASL	"B"	Nitrogen
5	(1) SMOBC/HASL	"C"	Air
6	(1) SMOBC/HASL	"C"	Nitrogen
7	(2) OSP	"A"	Air
8	(2) OSP	"A"	Air
9	(2) OSP	"B"	Nitrogen
10	(2) OSP	"B"	Air
11	(2) OSP	"C"	Nitrogen
12	(2) OSP	"C"	Air
13	(3) ENIG	"A"	Nitrogen
14	(3) ENIG	"A"	Air
15	(3) ENIG	"B"	Air
16	(3) ENIG	"B"	Nitrogen
17	(3) ENIG	"C"	Air
18	(3) ENIG	"C"	Nitrogen
19	(4) Matte Sn	"A"	Air
20	(4) Matte Sn	"A"	Nitrogen
21	(4) Matte Sn	"B"	Air
22	(4) Matte Sn	"B"	Air
23	(4) Matte Sn	"C"	Nitrogen
24	(4) Matte Sn	"C"	Air
25	(5) Imm. AG	"A"	Nitrogen
26	(5) Imm. AG	"A"	Air
27	(5) Imm. AG	"B"	Nitrogen
28	(5) Imm. AG	"B"	Air
29	(5) Imm. AG	"C"	Air
30	(5) Imm. AG	"C"	Nitrogen

Solder paste prints were made using a 0.006" thick stainless steel laser cut, electropolished stencil. Ten percent aperture reductions were used on the fine pitch devices. PWBs were assembled at Schneider Electric on their assembly line consisting of an MPM AP-25 screen printer, Siemens S20 and F5 placement equipment and a BTU Pyramax 98N Reflow Oven with Air and Nitrogen capability supplied by BTU International for this experiment. The Schneider plant maintains a Relative Humidity (RH) level between 35-40%.

After reflow, PWBs were packaged in ESD bags and taken to M/A-COM where two University of Massachusetts – Lowell senior students visually inspected the solder joints based on training by a certified IPC inspector / trainer. Inspection criteria were established as follows: Total Defects, Cold Solder joints, Non-wetting, Solder Balls, Dewetting, Bridging, Pinholes, Shiny Appearance, Smooth Appearance, and Flux Residue. X-ray radiography of the BGA solder joints was also performed. Initial inspection data has been tabulated and statistically analyzed by UML and Air Products. These results were published in prior papers at the SMTI and APEX conferences in 2003.

Figure 1. Test Vehicle

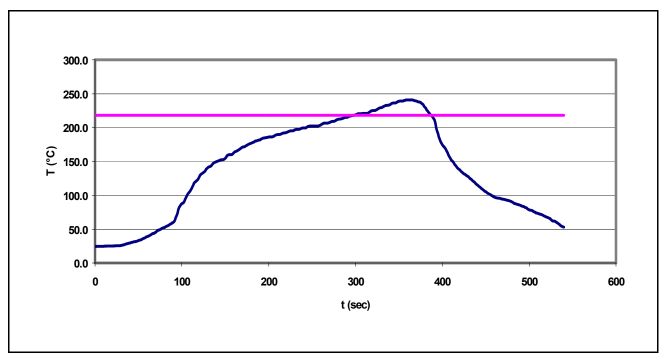


Figure 2. Reflow Profile for SMT Board Assembly

Visual analysis results, phase II

The major difficulties encountered in assembly were with stencil printing and placement system vision. In spite of using print parameters close to those in the application notes supplied for the three pastes, paste A had a tendency to adhere to the sides of the stencil openings. This resulted in scant prints on some of the fine pitch apertures. Paste B clogged the stencil severely; necessitating cleaning after every four or five prints. Paste C performed as expected with little difficulty. All three pastes exhibited good tack or component holding qualities during and after placement.

Visual defects statistical analysis, phase II
Eight main categories of common defects were selected and all boards were inspected. Those defects observed were photographed and recorded. Statistical analyses were performed using Minitab and significant effects were determined (Table 2). Ms. Pasquito trained the UML students to inspect the PWBs according to the latest available methods and IPC 610C inspection standards.

Table 2. Statistical Analysis – Total Visual Defects

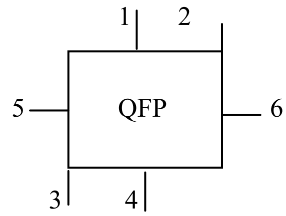
Source	DF	SS	MS	F	Pr > F
PWB Finish	4	44.7	11.2	7.33	0.0003
Solder	2	79	39.5	25.91	<.0001
Atmosp	1	132.4	132.4	86.88	<.0001
Finish *Solder	8	16.04	2.00	1.32	0.2735
Finish* Atmop	4	15.3	3.8	2.51	0.0629
Solder *Atmop	2	54.3	27.2	17.83	<.0001
Finish * Solder *Atmp	8	21.8	2.7	1.79	0.1184
Total	59	409.20			

As seen above, the ANOVA (Analysis of Variance) is significant for the overall experiment and for the variables highlighted with probabilities (Pr) less then .05.

Further statistical analysis of visual defects indicated the following conclusions:

1. The PWB Finish SMOBC/HASL significantly differs (worse) from other finishes. The remaining 4 finishes were indistinguishable from each other.
2. All Pastes were found to differ significantly. B performed best, but clogged stencils. In later tests in phase III, B vendor solved this problem
3. Nitrogen preformed significantly better than Air
4. Only in the case of solder paste B; was it shown that there is no significant difference between the use of air or nitrogen. The other two solders required nitrogen to reach the same level of visual quality as B
5. There were not enough data points to analyze the differences, if any in visual defects between the two levels of nitrogen (50 ppm versus 5000 ppm oxygen).

Pull tests prior to thermal cycling, phase II
The test methodology consisted of using an Instron pull test machine to pull the leads of an IC and record the maximum pull force. The pull tests were analyzed separately for each type of IC because of the differences of pad size and component finish. For the QFP (NiPdAu) components leads, six (6) leads were pulled as follows (Figure 3), and for the SOIC 20 (NiPdAu)) and the SOIC 16 (matte tin) leads, four (4) leads were pulled (Figure 4).



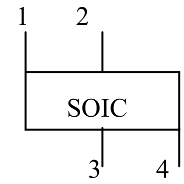


Figure 3. Position of QFP Pulls **Figure 4.**SOIC Pulls

The process of pulling the leads was:

1. The PCB is loaded at 45' to the Instron machine and affixed with 6 screws to a specially designed hold down fixture, shown in Figure 1.
2. The leads adjacent the ones that were pulled were removed (clipped) to facilitate pulling of target leads
3. The leads that were pulled were tied with a wire loop right through the IC's leads. Music wire (0.016"Diameter) was used for QFP, and fishing line (#24lb test) was used for SOIC.
4. A new loop was made for each IC pulled
5. The pull rate was 1" per minute, noting down the peak pull force.
6. The fractures were inspected and failure mode for each pull was noted.

Two (2) PWBs were unable to be pulled because of improper reflow in one case and severe bending in the other.

Summary pull test before thermal cycling, phase II
The pull test results before thermal cycling were analyzed including these important conclusions:

I The selection of materials and process affects the pull strength of the solder joints for the QFP and SOIC components tested, using components with NiPdAu finish:

1. Pull forces are dependant on the PWB pad size and footprint of the components used Thus pull forces on SOIC were higher that QFP.
2. PWB surface finish has a significant effect on the pull test of the leads. Of the five PWB finishes, ENIG was significantly lower than the other finishes in both IC's pulled. OSP was significantly higher in QFP and SMOBC/HASL was significantly higher in SOIC. ENIG pull test became non significance after thermal cycling.
3. Solder suppliers were not important in the pull tests for the two IC types. B was slightly higher in QFP and significantly higher in SOIC 20.
4. Pull strength for nitrogen was significantly higher than air for QFP, not significant for SOIC.

II Comparison of unleaded solder to leaded solder pull strength in QFP and SOIC, using components with NiPdAu finish.

This comparison was difficult since the baseline leaded PWBs were made with a single process from supplier B.

Analysis indicated that the difference is not significant in most cases when using solder supplier (B).

III Interchangeability of leaded and unleaded components and solders in SOIC and tin plated components pull tests.

This is an important issue for electronic component suppliers and customers, concerned about keeping a dual set of materials for different markets around the world as the technology transitions from leaded to lead-free soldering. The data for all test conditions analyzed, there is no significant difference in the pull test results.

Thermal cycling profile

The thermal profile selected for temperature cycling lead-free solder joints will have to be selected depending on these varying parameters.

- Maximum and minimum temperature. 0° and 100° C
- Ramp rates (up and down) for Min/maximum temperature. Select the fastest possible rates to increase the effects of low cycle fatigue and creep = 10°C/min.
- Dwell times at high and low temperatures. These are the shortest time for the solder joint system to stabilize prior to reversing the temperature = 20 minutes.
- Number of cycles. This number should be balanced between the reasonable times required to show deterioration of the solder joints versus the possibility of hard failures. It was decided to visually inspect the joints for cracks every 200 hours and to perform another pull test after 2000 cycles.
- No humidity or power cycling were performed.

The temperature profile is shown in Figure 5.

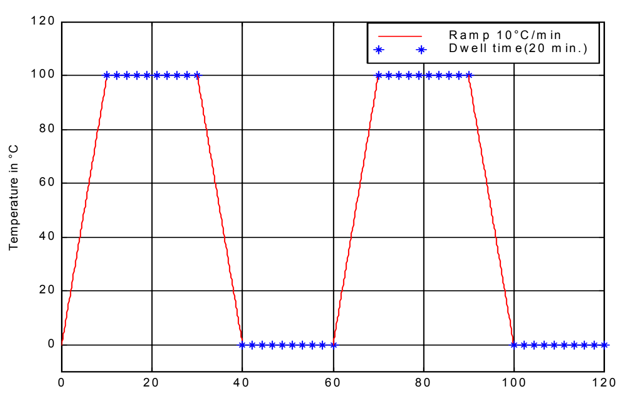


Figure 5. Thermal Profile for Reliability Testing of Lead-free Soldering

Post thermal cycling pull tests, phase II

The results of pull tests after 2000 iterations of thermal cycling are shown in Figure 6. Results were divided into 4 groups, in 2 sets (QFP and SOIC), both with NiPdAu. Components were compared under different PWB surface conditions, solder suppliers and atmospheres.

Based on the interaction table in Figure 6 and the ANOVA analysis (not shown) for QFP pulls post cycling:

- There is Significance among all main effects (surface finish, solders and atmosphere) as well as 1 interaction (solder x atmosphere due to solder 1).
- Variations in surface finish interactions are within the error because they are insignificant. Only HASL performs significantly lower than the rest of the surface finishes for all solder and atmosphere conditions.
- Soldering in Nitrogen generally gives better results in pull tests, Immersion Silver showed no improvement with nitrogen.
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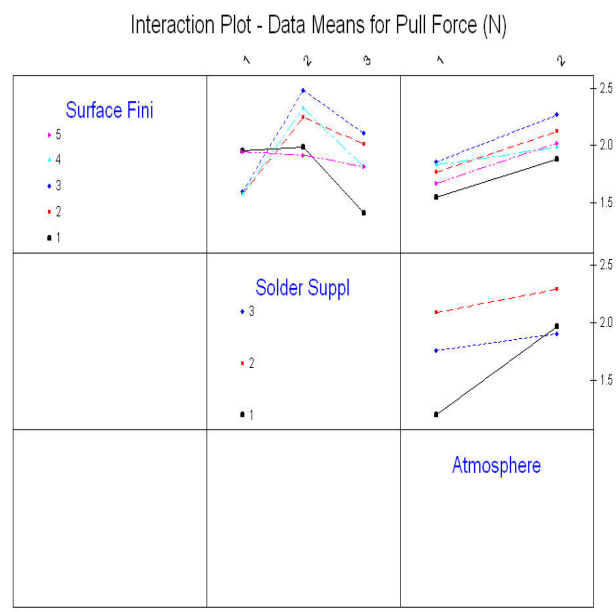

Figure 6. Interaction Plots of QFP ICs with NiPdAu pull tests after thermal cycling.

T tests were made of leaded vs. unleaded solders (supplier B) and the same surface finishes are shown in Table 3. Results indicate no difference between the lead-free PWBs and their leaded base, with other factors constant.

Conclusions of pull test for QFP's, phase II

When using NiPdAu finish and examining all 3 factors and their levels as well as conditions of leaded vs. unleaded and before vs. after cycling:

- Thermal cycling is significant for pull tests in most cases (23 out of 30 had lower pulls after).
- 2 surface finishes are significantly different in all cases (HASL and OSP). 3 surface finishes (ENIG, tin and immersion silver) are equivalent
- Under certain conditions, nitrogen and some solder suppliers are not significant
- When using same B solder supplier and air, leaded and unleaded solders are equivalent.

Table 3. T-test comparison of leaded and un-leaded solder pull tests after cycling for QFP/ NiPdAu finish, comparing 4 experiments of the same factors/levels

Exp #	Surface Finish	BSolder Supplier	Atm	Comp Finish	P 2 Tailed	Prob %
3	HASL	Pb-Free	Air	Pb-Free		
31	HASL	Leaded	Air	Leaded	0.19	19.40
9	OSP	Pb-Free	Air	Pb-Free		
32	OSP	Leaded	Air	Leaded	0.68	68.33
15	ENIG	Pb-Free	Air	Pb-Free		
33	ENIG	Leaded	Air	Leaded	0.94	93.99
21	Matte Sn	Pb-Free	Air	Pb-Free		
34	Matte Sn	Leaded	Air	Leaded	0.13	13.26

The same analysis was performed (Table 4) for SOIC ICs with NiPdAu component finish.

Table 4 – T-test comparison of leaded and unleaded solders pull tests after cycling for SOIC/ NiPdAu finish, comparing 4 experiments of the same factors/levels

Exp #	Surface Finish	BSolder Supplier	Atm	Comp Finish	P 2 Tailed	Prob %
3	HASL	Pb-Free	Air	Pb-Free		
31	HASL	Leaded	Air	Pb-Free	0.98	97.92
9	OSP	Pb-Free	Air	Pb-Free		
32	OSP	Leaded	Air	Pb-Free	0.71	71.11
15	ENIG	Pb-Free	Air	Pb-Free		
33	ENIG	Leaded	Air	Pb-Free	0.02	1.74
21	Matte Sn	Pb-Free	Air	Pb-Free		
34	Matte Sn	Leaded	Air	Pb-Free	0.66	66.01

Conclusions of pull test for SOIC, phase II

For SOICs with Tin Component finish, no statistical differences whether leaded or lead free with all factors and levels, using solder supplier B and air.

For SOICs with NiPdAu finish

- Thermal cycling is not significant for pull tests.
- 2 Surface finishes were borderline significant prior to cycling (HASL/Higher and ENIG/lower) But all surface finishes are equivalent after
- Only the solder suppliers are significantly different (surface finish and nitrogen are not significant)
- Results did not change statistically after thermal cycling, regardless of solder supplier
- Only ENIG changed statistically (better) between leaded and unleaded boards, when using B solder supplier and reflowed in air. Note that in pull tests prior to thermal cycling, ENIG was significantly lower than the rest, shown earlier.

Further research and phase III testing of lead-free soldering

Phase III testing of the lead-free consortium research will focus on examining the manufacturing issues of lead-free implementation in production. Prior results of work done at the consortium as well as other published research will be incorporated into the material and process selection of lead-free testing. New consortium members were added to provide resources and background to volume production application of lead-free. These companies will provide valuable knowledge and material contribution of mass market volume applications. The research will be sponsored by EPA under work order 4W-1362-NAEX. The project has progressed with the following decisions:

- *Factors and levels of the phase III experiment:*

The following factors were selected based on the results of phase II and the collective experience of the consortium members: 2 lead free solder paste suppliers, 3 surface finishes and 2 types of PWB lamination cycles, single or double, shown on table 5. Other factors such as laminate material (FR4), 0-3-6 thermal cycle for the laminate; solder reflow profile (as recommended by the supplier) and atmosphere (air) were fixed based on members' consensus. Each PWB will undergo 3 reflows in assembly; one for the top component side, another for the reverse (bottom) side and a third to simulate rework.

Table 5: Phase 3 Lead Free Solder Test Plan

Experiment #	Surface Finish	Solder paste	Lamination Cycles
1	(1) Imm Ag	"A"	Single
2	(1) Imm Ag	"A"	Double
3	(1) Imm Ag	"B"	Single
4	(1) Imm Ag	"B"	Double
5	(2) OSP	"A"	Single
6	(2) OSP	"A"	Double
7	(2) OSP	"B"	Single
8	(2) OSP	"B"	Double
9	(3) ENIG	"A"	Single
10	(3) ENIG	"A"	Double
11	(3) ENIG	"B"	Single
12	(3) ENIG	"B"	Double

- *Baseline leaded solder experiments*

To reduce the number of iterations, 3 finishes and 2 solder pastes were used to provide the lead free baseline experiments as shown in Table 6. Double lamination was chosen for all leaded baseline experiments because it is more robust.

- *Component finishes*

A variety of component finishes will be used in the test PWB. They include: NiPdAu, Sn, SnPb, Au, Ni-Au, Sn/Ni, SnAgCu, and matte Sn. Some components will be available in daisy chain configurations.

Table 6: Leaded Solder Baseline Test Plan, Phase III

Experiment #	Surface Finish	Leaded Solder paste	Lamination Cycles
1	(1) Imm Ag	"A"	Double
2	(1) Imm Ag	"B"	Double
3	(2) OSP	"A"	Double
4	(2) OSP	"B"	Double
5	(3) ENIG	"B"	Double
6	(3) ENIG	"B"	Double

- *Proposed test methodology for phase III*

Initially, all PWBs will be tested right after the reflow process using a coupon for IST (interconnect stress test) to evaluate the higher temperature effects on lamination.

100% visual tests will be performed on all solder joints based on IPC inspection standard 610D, as well as simulated reliability tests.

The reliability tests will be divided evenly, between the thermal cycling performed in phase II and a new HALT testing on the other half of the PWBs. Pull tests will be performed prior and after thermal cycling and HALT testing.

It is estimated that the results of the testing will be available in summer 2005.

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- Tom Bzik of the Statistical Science Group, Air Products, for statistical analysis and discussions.
- Raytheon Company Reliability group for providing the expertise and the oven for thermal cycling of the PWB's.

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